IN THE SPECIFICATION:

Please amend the specification as follows:

[0054] After formation of the spacers 25, semiconductor material 26 is formed on the exposed surface of the second semiconductor layer 12 providing the structure shown, for example, in FIG. 4E. As with the straining layer ~~21~~ 23 discussed above, a straining layer 41 can also be utilized with this embodiment. The properties of both straining layers would be similar. The structure illustrated in FIG. 4E is then planarized to provide the substantially planer structure shown in FIG. 4F. Note that the planarization step removes the nitride mask 20 and the surface dielectric layer 18 that were not previously etched so as to provide a structure in which first semiconductor layer 16 is exposed and regrown semiconductor material 26 is exposed. The exposed first semiconductor layer 16 is the region in which a first semiconductor device such as an NFET will be formed, whereas the exposed surface of semiconductor material 26 is the region in which a second semiconductor device, such as a PFET, will be formed.